ICEM Generator – A tool for the construction of IC emission models

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Context – EMC simulation CEM of electronic equipments

 Needs: Predict by simulation EMC performances (emission, immunity) of electronic equipments, compliance to EMC requirements, analyze EMC issues and optimize countermeasures.

« Divide and Conquer » approach - independent modeling and interconnection of the subparts of the system

Extraction of the models by simulation, measurement or data from manufacturer
Obstacles for EMC modeling of ICs:

- Complex circuits → model order reduction, macromodeling approach

- Extraction by measurement is a difficult task (large number of access and power domains)

- Confidential information: IC manufacturers provide few information about the internal structure of their ICs
**Context – ICEM**

Integrated Circuit Emission Model (ICEM) standard (IEC62433-2) for conducted emission modeling of IC at PCB level.

**Principle:**

- **Passive Distribution Network** (power distribution network at die and package level, independent of IA)
- **Internal Activity** (charge transfer due to IC switching).

- Limit: few manufacturers deliver ICEM of their circuit
- Is it possible for an IC end-user to build ICEM model?

<table>
<thead>
<tr>
<th></th>
<th>Measurement-based approach</th>
<th>Simulation-based approach</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PDN</strong></td>
<td>✔ State-of-the-art</td>
<td>✔ Extraction of package model by electromagnetic simulation ✔ Evaluation of die PDN</td>
</tr>
<tr>
<td><strong>IA</strong></td>
<td>✖ One method proposed by IEC62433-2 but accuracy issues for complex devices ✔ Extraction of a model valid for only one configuration</td>
<td>✖ Design information required ✔ Rough evaluation from simple technological information, but influence of configuration is not taken into account</td>
</tr>
</tbody>
</table>
ICEM Generator tool

- Purpose: dedicated to IC end-users to:
  - Build a first version of ICEM model with a reasonable accuracy
  - Integrate the influence of the actual configuration of the circuit
  - Rapid extraction, without optimization process by measurement vs. simulation comparison

- Principle of the approach
  - Required information: dynamic power consumption.
  - Generic parameter for electronic designer, numerous design tool to evaluate power.
  - This parameter is not mentioned by ICEM standard.

**Dynamic current consumption profile of a digital circuit (« Activity »)**

\[
P_{_{\text{dyn}}} = \frac{1}{T} \int_{0}^{T} i_{\text{dyn}}(t) dt
\]
Prototype designed for the extraction of the « core » model of a FPGA from Xilinx

Algorithm based on Chaimae Ghfiri PhD

Use the reports from post placement & routing synthesis, vectorless simulation

**Simulation flow for FPGA**

- Post P&R synthesis (.pwr file, .twr file)
- ICEM generator
- ICEM
  - SPICE simulator
  - Conducted emission simu.
- PCB, cables, passives models
Case study description

✓ Xilinx Spartan6 XC6SLX9-2FT256 FPGA mounted on a test board for EMC measurement according to IEC61967

✓ Synthesized application:
  - Real-time filtering and FFT
  - Frequency = 16 MHz
  - Used on-chip resources:
    • 1792 CLB
    • 4 Block RAM
    • 1 DCM
    • 30 DSP blocks
  - Total power = 49 mW
EMC simulation flow

- Package Z(f) meas.
- ICEM – PDN (equiv RLC circuit)
- PCB model (Black-box model)
- PCB routing file (Gerber)
- ICEM - IA

SPICE simulator

Schematic diagram

Conducted emission simu.
Full electrical model

PCB model

ICEM-IA block
(extracted from ICEM generator)

Measurement receiver model

ICEM-PDN block
Results

Power integrity

Contribution CLB

Contribution clock + DCM

Emission conduite

Peak-to-peak amplitude:
- Measurement: 16 mV
- Simulation: 14.6 mV

RMS error = 5.6 dB
Results

✓ Comparison with IA extraction method proposed by ICEM ("standard method")

IA profiles

Conducted emission (150 Ω)

Dynamic power:
✓ Measurement: 24 mW
✓ IA std method: 40 mW
✓ IA new method: 23 mW

RMS error:
✓ IA std method: 13.4 dB
✓ IA new method: 8.9 dB
Conclusion

- Development of a software tool to help end-users to build ICEM model of IC (IA core block)

- Advantages:
  - rapid estimation with acceptable accuracy
  - IA construction independent on PDN construction (weakness of method proposed by ICEM standard)
  - IC configuration dependent model

- Perspectives:
  - Include I/O noise
  - Extend to other FPGA family and manufacturers
  - Extend to other class of Ics (SoC, low-power microcontroller)
  - Add rapid estimation tool of PDN and IA
  - Statistical approach to evaluate margin of error
Thank you for your attention